II. Listing of Claims

1. (Currently Amended) A method for providing an alternative reference description for the use in verification of digital circuits by using a computer, wherein in the verification a digital circuit to be verified is compared with a reference description of the digital circuit, in order to recognize errors in the digital circuit using an equivalence test, wherein for at least one specific circuit structure described by a reference description of the digital circuit a plurality of different pre-defined implementation alternatives is known, the method comprising the computer implemented steps of:

(a) determining, for each one of the at least one specific circuit structure first implementation alternative out of the plurality of the different pre-defined implementation alternatives, such that the first implementation alternative has the greatest degree of structural equivalence with the digital circuit to be verified compared to other implementation alternatives out of the plurality of the different pre-defined implementation alternatives and whereby each one of the plurality of the different pre-defined implementation alternatives is simulated respectively, using random pattern simulation, and compared with a corresponding simulation of the digital circuit, in order to determine the first implementation alternative having the ~~greatest~~ highest degree of structural equivalence with the digital circuit, the implementation alternative out of the plurality of the different pre-defined implementation alternatives, which, under the random pattern simulation, has the largest number of equivalent design points with the digital circuit,

(b) replacing in the reference description of the digital circuit, the description of the individual circuit structures by the first implementation alternative determined for the respective circuit structure in step (a) having the ~~greatest~~ highest degree of structural equivalence in each case to obtain the alternative reference description, and

(c) outputting the alternative reference description for use as a reference description in the verification of the digital circuit,

wherein the at least one specific circuit structure, for which in step (a) the first implementation alternative with the highest degree of structural

equivalence is determined in each case, are multiplier structures for realizing integral multiplication functions.

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Previously Presented) The method according to claim 1, wherein the reference description is selected from a group comprising RTL-, VHDL- and Verilog-descriptions.

6. (Previously Presented) The method according to claim 1, wherein an equivalence test is executed by comparing an existing implementation of the digital circuit with the alternative reference description.

7. (Previously Presented) The method according to claim 1, wherein the plurality of different pre-defined implementation alternatives for the specific circuit structures comprise varying architectures of the specific circuit structures aided by a synthesis device available for the design of the digital circuit.

8. (Cancelled)

9. (Previously Presented) The method according to claim 1, wherein in step (a) for each circuit structure, the different implementation alternatives are simulated at the same time and compared with the simulation of the digital circuit.

10. (Previously Presented) The method according to claim 9, wherein the different implementation alternatives for each circuit structure are simulated at the same time by inputs of the implementation alternatives being connected with one another and corresponding outputs of the implementation alternatives being led to a common output to maintain the circuit function of the individual implementation alternatives.

11. (Previously Presented) The method according to claim 10, wherein the outputs of the different pre-defined implementation alternatives are connected by a logic OR link to the common output.

12. (Previously Presented) The method according to claim 1, wherein for each implementation alternative in step (a), the degree of equivalence with the simulation of the digital circuit is obtained by the number of values output for individual simulation patterns of the reference description with the respective implementation alternative, the alternative values identically output, which are identical to values output by the digital circuit for the corresponding simulation patterns, being determined for the simulation patterns for each implementation alternative and being used as degree of equivalence for the corresponding implementation alternative.

13. (Previously Presented) The method according to claim 1, wherein determining the first implementation alternatives with the greatest degree of structural equivalence carried out in step (a) is at least partially performed by a method of equivalence class refinement, wherein all internal design points, whose non-match has not yet been proven, are combined in an equivalence class.

14. (Currently Amended) ~~A device~~ An apparatus for providing an alternative reference description for the use in verification of digital circuits,

with first memory means for storing a description of a digital circuit to be verified,

with second memory means for storing a reference description of the digital circuit, and

with verification means, which are set up in such a manner that the verification means compare the description of the digital circuit to be verified with the reference description, in order through an equivalence test to recognize errors in the digital circuit,

wherein third memory means are provided for storing a plurality of different pre-defined implementation alternatives for at least one specific circuit

structure of the digital circuit, whereby the verification means are set up in such a manner that, for each one of the at least one specific circuit structure, the verification means determine a first implementation alternative out of the plurality of different pre-defined implementation alternatives, such that the first implementation alternative has the greatest degree of structural equivalence with the digital circuit to be verified, compared to other implementation alternatives out of the plurality of the different pre-defined implementation alternatives,

the verification means are set up in such a manner that, for determining the first implementation alternative out of the plurality of different pre-defined implementation alternatives that has the greatest degree of structural equivalence with the digital circuit in each case, the verification means simulate each one of the plurality of different pre-defined implementation alternatives respectively, using random pattern simulation, and compare the simulations with a corresponding simulation of the digital circuit, to determine the first implementation alternative with the greatest degree of structural equivalence with the digital circuit, which under the random pattern simulation, has the largest number of equivalent design points with the digital circuit, and

the verification means are set up in such a manner that the verification means insert the previously determined first implementation alternatives with the greatest degree of structural equivalence, respectively, in the reference description of the digital circuit to obtain the alternative reference description for the individual specific circuit structures and output the alternative reference description for use as a reference description in the verification of the digital circuit,

wherein at least one specific circuit structure, for which in step (a) the first implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures for realizing integral multiplication functions.

15. (Currently Amended) The ~~device~~ apparatus according to claim 14, wherein, the device is adapted to execute a method for the verification of digital circuits, wherein a digital circuit to be verified is compared with an alternative reference description of the digital circuit, in order, to recognize errors in the digital circuit using an equivalence test, wherein for at least one specific circuit structures described by a reference description of the digital circuit, a plurality of different pre-

defined implementation alternatives is known, the method comprising:

(a) determining, for each one of the at least one specific circuit structure first implementation alternative out of the plurality of the different pre-defined implementation alternatives, such that the first implementation alternative has the greatest degree of structural equivalence with the digital circuit to be verified compared to other implementation alternatives out of the plurality of the different pre-defined implementation alternatives, and whereby each one of the plurality of the different pre-defined implementation alternatives is simulated respectively, using random pattern simulation, and compared with a corresponding simulation of the digital circuit, in order to determine the first implementation alternative having the greatest degree of structural equivalence with the digital circuit, the implementation alternative out of the plurality of the different pre-defined implementation alternatives, which, under the random pattern simulation, has the largest number of equivalent design points with the digital circuit,

(b) replacing in the reference description of the digital circuit, the description of the individual circuit structures by the first implementation alternative determined for the respective circuit structure in step (a) having the greatest degree of structural equivalence in each case to obtain the alternative reference description, and

(c) outputting the alternative reference description for use as a reference description in the verification of the digital circuit,

wherein at least one specific circuit structure, for which in step (a) the first implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures for realizing integral multiplication functions.

16. (Currently Amended) A computer-program product with a program-code stored on a data medium, for executing a method for providing an alternative reference description for the use in verification of digital circuits, wherein in the verification a digital circuit to be verified is compared with a reference description of the digital circuit, in order, to recognize errors in the digital circuit using an equivalence test, wherein for at least one specific circuit structure described by a reference description of the digital circuit a plurality of different pre-defined

implementation alternatives is known, the method ~~comprising~~ comprises when executed on a computer:

(a) determining, for each one of the at least one specific circuit structure first implementation alternative out of the plurality of the different pre-defined implementation alternatives, such that the first implementation alternative has the greatest degree of structural equivalence with the digital circuit to be verified compared to other implementation alternatives out of the plurality of the different pre-defined implementation alternatives and whereby each one of the plurality of the different pre-defined implementation alternatives is simulated respectively, using random pattern simulation, and compared with a corresponding simulation of the digital circuit, in order to determine the first implementation alternative having the greatest degree of structural equivalence with the digital circuit, the implementation alternative of the plurality of the different pre-defined implementation alternatives, which, under the random pattern simulation, has the largest number of equivalent design points with the digital circuit,

(b) replacing in the reference description of the digital circuit, the description of the individual circuit structures by the first implementation alternative determined for the respective circuit structure in step (a) having the greatest degree of structural equivalence in each case to obtain the alternative reference description, and

(c) outputting the alternative reference description for use as a reference description in the verification of the digital circuit,

wherein at least one specific circuit structure, for which in step (a) the first implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures for realizing integral multiplication functions.

17. (Currently Amended) A digital storage medium with electronically readable control signals, which can cooperate with a computer system, executing a method for providing an alternative reference description for the use in verification of digital circuits, wherein in the verification a digital circuit to be verified is compared with a reference description of the digital circuit, in order, to recognize errors in the digital circuit using an equivalence test, wherein for at least one specific circuit

structure described by a reference description of the digital circuit a plurality of different pre-defined implementation alternatives is known, the method comprising:

(a) determining, for each one of the at least one specific circuit structure first implementation alternative out of the plurality of the different pre-defined implementation alternatives, such that the first implementation alternative has the greatest degree of structural equivalence with the digital circuit to be verified compared to other implementation alternatives out of the plurality of the different pre-defined implementation alternatives, and whereby each one of the plurality of the different pre-defined implementation alternatives is simulated respectively, using random pattern simulation, and compared with a corresponding simulation of the digital circuit, in order to determine the first implementation alternative having the greatest degree of structural equivalence with the digital circuit, the implementation alternative out of the plurality of different pre-defined implementation alternatives, which, under the random pattern simulation, has the largest number of equivalent design points with the digital circuit,

(b) replacing in the reference description of the digital circuit, the description of the individual circuit structures by the first implementation alternative determined for the respective circuit structure in step (a) having the greatest degree of structural equivalence in each case to obtain the alternative reference description, and

(c) outputting the alternative reference description for use as a reference description in the verification of the digital circuit,

wherein at least one specific circuit structure, for which in step (a) the first implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures for realizing integral multiplication functions.